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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,218	08/16/2005	Klaus Breitschwerdt	10191/3828	2649

26646 7590 07/06/2007
KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER

ARMAND, MARC ANTHONY

ART UNIT	PAPER NUMBER
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2814

MAIL DATE	DELIVERY MODE
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07/06/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/520,218	Applicant(s) BREITSCHWERDT ET AL.	
	Examiner Marc-Anthony Armand	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 August 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 22-45 and 51 is/are pending in the application.
- 4a) Of the above claim(s) 46-50 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 22-45 and 51 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 January 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>01/03/2005</u> . | 6) <input type="checkbox"/> Other: _____ |

N.A.

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DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 22-45 and 51 in the reply filed on April 19, 2007 is acknowledged.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
 2. Ascertaining the differences between the prior art and the claims at issue.
 3. Resolving the level of ordinary skill in the pertinent art.
 4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
3. **Claims 22-30,39,43,44,51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Geusic et al., (Geusic) USPAT 6,198,168 in view of Wen et al., (Wen) USPAT 6,207,903.**

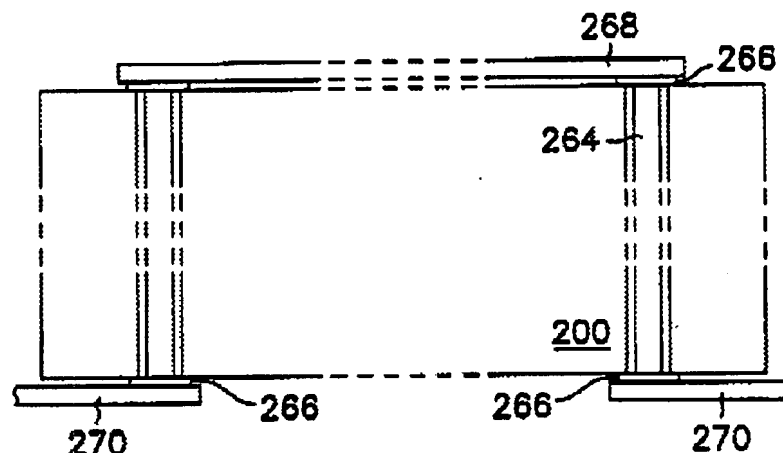


FIG. 8

As per claims 22, 24, Geusic shows in fig. 8 and discloses (col.5, line 60-68) and (col.6, line 1-10) an electrical component, having a first metallization layer (268) (applicant's conductive structure); a second conductive structure (270); at least one via (264) (applicant's feedthrough); a substrate (applicant's base element) provided with at least one via (268) (applicant's feedthrough) that connects the first conductive structure (268), the first conductive structure extending on or in a vicinity of an upper side of the base element (200), to the second conductive structure (270), the second conductive structure (270) extending on or in a vicinity of a lower side of the base element (200) and includes a first conductive structure (268) and a second conductive structure (270).

Geusic differs from the claimed invention because he does not explicitly disclose an electronic device having a right prism or a right cylinder, also a planar waveguide that can be used for high-frequency electromagnetic waves.

Wen discloses (col.3, line 10-55) a coplanar waveguide that can be used for high-frequency electromagnetic waves (col.3, line 1-10); vias (22) in fig.3b that includes one of a right prism and a right cylinder.

Wen is evidence that an ordinary skilled in the art would find a reason, suggestion or motivation to have a coplanar waveguide that can be used for high-frequency electromagnetic waves and vias including one of a right prism and a right cylinder; and also he discloses (col.1, line 23-28) that it will provide a device with an improve device and an improve via interconnects. Therefore, it would have been obvious to a person having ordinary skills in the art to incorporate the coplanar waveguide at the time the invention was made, teaching of Wen in Geusic's electrical component in order to provide an improved device and also an improved via interconnects or intended use as taught by Wen in (col.3, line 1-10) and (col.1, line 23-28).

As per claim 23, Wen discloses (col.3, line 10-55) an electrical component where the electrical component is one of a high-frequency micromachined (applicant's microelectromechanical component).

As per claim 25, Geusic shows in fig. 8 and discloses (col.5, line 60-68) and (col.6, line 1-10) that the electrical component has at least one via (applicant's feedthrough) is one of filled and lined with an electrically conductive material corresponding to a metal.

As per claim 26, Geusic shows in fig. 8 and discloses (col.5, line 60-68) and (col.6, line 1-10) that the electrical component has the substrate (200) (applicant's base element) that is flat at least in a vicinity of the at least one via (applicant's feedthrough), and the at least one feedthrough extends perpendicularly to a plane spanned by the vicinity of the base element that is flat and penetrates through the substrate (200) (applicant's base element).

As per claim 27, Geusic shows in fig. 8 and discloses (col.5, line 60-68) and (col.6, line 1-10) that the electrical component has at least one via (264) (applicant's feedthrough) with a conductive material.

As for the process "etching " and "plasma etching" and "filled" do not carry weight in a claim drawn to a structure. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by- process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777F, 2d 659, 698, 227 USPQ 964, 966 (Fed. Cir. 1985); see also MPEP 2113.

As per claim 28 Geusic shows in fig. 8 and discloses (col.5, line 60-68) and (col.6, line 1-10) that the electrical component has at least one via (applicant's feedthrough) that is rectangular in plan view.

As per claim 39, Geusic shows in fig. 8 and discloses (col.5, line 60-68) and (col.6, line 1-10) that the electrical component having vias (264) and conductive structures, a first vias (264) (applicant's feedthrough), a second feedthrough (264), and a third feedthrough (264)

Geusic differs from the claimed invention because he does not explicitly disclose an electronic device having a first conductive structure includes an upper coplanar waveguide having a first upper ground lead, an upper signal lead, and a second upper ground lead, the first upper ground lead, the upper signal lead, and the second upper ground lead extending at least locally parallel to one another, the second conductive structure includes a lower coplanar waveguide having: a first lower ground lead, a lower signal lead, and a second lower ground lead, the first lower ground lead, the lower signal lead, and the second lower ground lead extending at least locally parallel to one another, the first upper ground lead is connected to the first lower ground lead by way of the first feedthrough, the second upper ground lead is connected to the second lower ground lead by way of the second feedthrough, the upper signal lead is connected to the lower signal lead by way of the third feedthrough, and the third feedthrough is offset with respect to the first feedthrough and the second feedthrough.

Wen discloses (col.3, line 10-55) and shows fig.1a and 1b an electronic device having a first conductive structure (12) that includes an upper coplanar waveguide having: a first upper ground lead, an upper signal lead, and a second upper ground lead, the first upper ground lead, the upper signal lead, and the second upper ground lead extending at least locally parallel to one another, the second conductive structure

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(14) that includes a lower coplanar waveguide having: a first lower ground lead, a lower signal lead, and a second lower ground lead, the first lower ground lead, the lower signal lead, and the second lower ground lead extending at least locally parallel to one another, the first upper ground lead is connected to the first lower ground lead by way of the first feedthrough, the second upper ground lead is connected to the second lower ground lead by way of the second feedthrough, the upper signal lead is connected to the lower signal lead by way of the third feedthrough, and the third feedthrough is offset with respect to the first feedthrough and the second feedthrough.

Wen is evidence that an ordinary skilled in the art would find a reason, suggestion or motivation to have an electronic device having a first conductive structure includes an upper coplanar waveguide having a first upper ground lead, an upper signal lead, and a second upper ground lead, the first upper ground lead, the upper signal lead, and the second upper ground lead extending at least locally parallel to one another, the second conductive structure includes a lower coplanar waveguide having: a first lower ground lead, a lower signal lead, and a second lower ground lead, the first lower ground lead, the lower signal lead, and the second lower ground lead extending at least locally parallel to one another, the first upper ground lead is connected to the first lower ground lead by way of the first feedthrough, the second upper ground lead is connected to the second lower ground lead by way of the second feedthrough, the upper signal lead is connected to the lower signal lead by way of the third feedthrough, and the third feedthrough is offset with respect to the first feedthrough and the second feedthrough and he also discloses that it will improve the RF impedance matching at the

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via transition. Therefore, at the time the invention was made, it would have been obvious to a person having ordinary skill in the art to have a ground-signal-ground on the conductors teaching of Wen with Geusic's device because it will improve the RF impedance matching at the via transition as taught by Wen in (col.3, line 37-39).

As per claim 43, Geusic shows in fig. 8 and discloses (col.5, line 60-68) and (col.6, line 1-10) that the electrical component has an electrical component provided on an upper side of the substrate (200) (applicant's base element) and capable of being electrically activated by way of the at least one via (264) (applicant's feedthrough) from the lower side of the substrate (200) (applicant's base element)

As per claim 44, Geusic shows in fig. 8 and discloses (col.5, line 60-68) and (col.6, line 1-10) that the electrical component has at least one vias (applicant's feedthrough).

Geusic differs from the claimed invention because he does not explicitly disclose that the electrical component has a short circuit switch for high –frequency electromagnetic waves.

Wen discloses (col.3, line 10-55) a coplanar waveguide that can be used for high-frequency microelectronic electromagnetic waves (col.3, line 1-10) having a short circuit switch for high-frequency electromagnetic waves.

Wen is evidence that an ordinary skilled in the art would find a reason, suggestion or motivation to have a short circuit switch for high-frequency electromagnetic waves; and also he discloses (col.1, line 23-28) that it will provide a device with an improve device and an improve via interconnects. Therefore, it would have been obvious to a person having ordinary skill in the art to incorporate the coplanar waveguide at the time the invention was made, teaching of Wen in Geusic's electrical component in order to provide an improved device and also an improved via interconnects or intended use as taught by Wen in (col.3, line 1-10) and (col.1, line 23-28).

As per claim 51, Wen discloses (col.3, line 10-55) and shows fig.1a and 1b that an electronic device is sued to create low-loss high-frequency crossovers (col.3, line 1-10).

As per claim 29 and 30, Geusic shows in fig. 8 and discloses (col.5, line 60-68) and (col.6, line 1-10) a via (264) with a width a diameter and also an area.

Geusic differs from the claimed invention because he does not explicitly disclose that at least one feedthrough occupies in plan view an area of $400 \mu\text{m}^2$ to $40,000 \mu\text{m}^2$, and the at least one feedthrough has a diameter of $20 \mu\text{m}$ to $200 \mu\text{m}$, in particular $40 \mu\text{m}$ to $100 \mu\text{m}$. and also, an area of $1,600 \mu\text{m}^2$ to $10,000 \mu\text{m}^2$, and the at least one feedthrough has a diameter of $40 \mu\text{m}$ to $100 \mu\text{m}$. It would have been an obvious matter of design choice to have a particular diameter and area for the via, since such a modification would have involved a mere

change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

As per claim 32, Wen discloses (col.1, line 30-36) that the electrical component has a base element that includes a high resistivity silicon substrate having a resistance.

Wen discloses the claimed invention except for the value the resistance value of the silicon disk. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to a particular resistance value for the silicon disk, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980). Also, the substrate (200) of the device of Wen is silicon which is the same material disclosed in the claimed invention

As per claim 31, Geusic discloses (col.3, line 55-60) that the base element has, in a region vias (264), a thickness of 500.mu.m.

As per claim 40, Wen discloses (col.3, line 10-55) that the electrical component has a plan view where the offset of the third via (13) (applicant's feedthrough) on the base element has a particular size.

Wen discloses the claimed invention except for a range for the size of the via that is from 50 .mu.m to 300 .mu.m. It would have been an obvious matter of design choice to have a particular range for the size of the via, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the

optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

As per claim 41, Wen discloses (col.3, line 10-55) that the electrical component has a plan view where the offset of the third via (13) (applicant's feedthrough) has a particular size.

Wen discloses the claimed invention except for value for the size of the via that is 150 m.u.m . It would have been obvious to one having ordinary skill in the art at the time of the invention was made to have a particular size for the via, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

6. Claims 33-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Geusic and Wen as applied to claim 1 above and further view of Nakao et al., (Nakao) USPAT 5,926,377.

As per claims 33 and 34,42 Geusic modify by Wen discloses an electronic component having a first and second conductive structure.

Geusic modify by Wen differs from the claimed invention because they do not explicitly disclose a dielectric separating the first and second conductive structure and also that the dielectric includes a pattern and also form an interdigital capacitor.

Nakao shows in fig.18 and discloses (Abstract) a first and second conductive layer (60) and (23) interposed by an insulating material and also that forms a pattern and also a capacitor. Nakao is evidence that an ordinary skilled in the art would find a reason, suggestion or motivation to have a first and second conductive layer interposed

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by an insulating material and also that forms a pattern and form a capacitor; and also he discloses (col.10, line 39-41) that it will provide a device that can reduce the emission of unwanted waves. Therefore at the time the invention was made, it would have been obvious to a person having ordinary skill in the art to have a have a first and second conductive layer interposed by an insulating material and also that forms a pattern and a capacitor because it will provide a device that can reduce the emission of unwanted waves as taught by Nakao in (col.1,line 40-44).

As per claims 35,36, Geusic modify by Wen and Nakao (col.5, line 15-20) discloses the claimed invention except for the range of the value of the capacitor. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the value of the capacitor within a range of .05pF to 4 pF, and 0.1pF to 2pF since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. Claims 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Geusic and Nakao as applied to claim 3 above and further view of Kanber (Kanber) USPAT 5,312,765

As per claims 37 and 38, Geusic modify by Wen discloses an electronic device having conductors and vias.

Geusic modify by Wen differs from the claimed invention because they do not explicitly disclose a dielectric that includes silicon oxide and also that has a thickness of 45nm to 1800 and 90nm to 900nm.

Kanber shows in fig.4 a microelectronic device having a silicon oxide layer as dielectric and also has a thickness.

Kander is evidence that an ordinary skilled in the art would find a reason, suggestion or motivation to have a silicon oxide layer as dielectric and also with a thickness; and also he discloses (col.4, line 25-30) that the dielectric will protect the device. Therefore at the time the invention was made, it would have been obvious to a person having ordinary skill in the art to have a silicon oxide layer as dielectric and also with a thickness because it will help protect the device as taught by kinder in (col.4, line 25-30).

As for the range of the thickness of the silicon oxide, that is within 45nm to 1800nm and 90nm to 900nm. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have a particular range for the thickness of the silicon oxide, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

8. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Geusic and Wen as applied to claim 22 above and further view of Imai (Imai) USPAT 5,901,050.

As per claim 45, Geusic modify by Wen discloses an electronic device having conductors and vias and a base element.

Geusic modify by Wen differs from the claimed invention because they do not explicitly disclose an electronic device having a hermetically sealed capsule.

Imai shows in fig.4 and discloses (col.6, line 20-66) a lid (22) (applicant's sealed capsule) sealed on the electronic device.

Imai is evidence that an ordinary skilled in the art would find a reason, suggestion or motivation to have lid covering the electronic device; and also he discloses (col.6, line 35-38) that the Lid will protect the device and facilitate the removal of heat from the circuit. Therefore at the time of the invention, it would have been obvious to a person of ordinary skill in the art to have a lid covering the device because it will help protect the device and facilitate the removal of heat from the circuit, as taught by Imai in (col.6, line 35-38).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

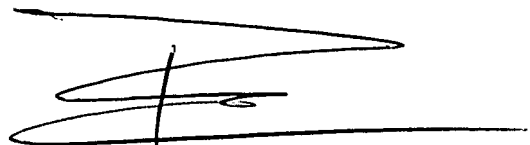
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marc-Anthony Armand whose telephone number is 571-272-9751. The examiner can normally be reached on Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Marc-Anthony Armand
Examiner
Art Unit 2814

M.A

A handwritten signature in black ink, consisting of a stylized 'T' followed by a horizontal line and a vertical stroke.

THAO X. LE
PRIMARY PATENT EXAMINER